Pm25LV512 / Pm25LV010

512 Kbit / 1 Mbit 3.0 Volt-only, Serial Flash Memory With 25 MHz SPI Bus Interface

FEATURES

• Single Power Supply Operation
- Low voltage range: 2.7 V - 3.6 V

• Memory Organization
- Pm25LV512: 64K x 8 (512 Kbit)
- Pm25LV010: 128K x 8 (1 Mbit)

• Cost Effective Sector/Block Architecture
- Uniform 4 Kbyte sectors
- Uniform 32 Kbyte blocks (8 sectors per block)
- Two blocks with 32 Kbytes each (512 Kbit)
- Four blocks with 32 Kbytes each (1 Mbit)
- 128 pages per block

• Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)

• High Performance Read
- 25 MHz clock rate (maximum)

• Page Mode for Program Operations
- 256 bytes per page

• Block Write Protection
- The Block Protect (BP1, BP0) bits allow part or entire of the memory to be configured as read-only.

• Hardware Data Protection
- Write Protect (WP#) pin will inhibit write operations to the status register

• Page Program (up to 256 Bytes)
- Typical 2 ms per page program time

• Sector, Block and Chip Erase
- Typical 40 ms sector/block/chip erase time

• Single Cycle Reprogramming for Status Register
- Build-in erase before programming

• High Product Endurance
- Guarantee 100,000 program/erase cycles per single sector (preliminary)
- Minimum 20 years data retention

• Industrial Standard Pin-out and Package
- 8-pin JEDEC SOIC
- 8-contact WSON
- Optional lead-free (Pb-free) packages

GENERAL DESCRIPTION

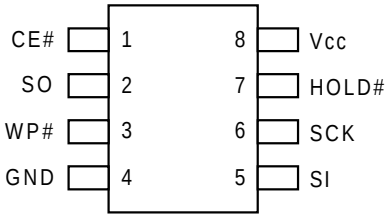
The Pm25LV512/010 are 512 Kbit/1 Mbits 3.0 Volt-only serial Flash memories. These devices are designed to use a single low voltage, range from 2.7 Volt to 3.6 Volt, power supply to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers as well.

The device is optimized for use in many commercial applications where low-power and low-voltage operation are essential. The Pm25LV512/010 is enabled through the Chip Enable pin (CE#) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All write cycles are completely self-timed.

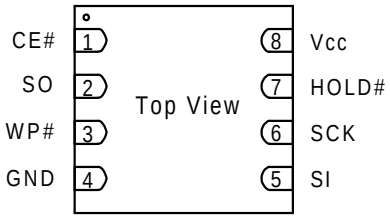
Block Write protection for top 1/4, top 1/2 or the entire memory array (1M) or entire memory array (512K) is enabled by programming the status register. Separate write enable and write disable instructions are provided for additional data protection. Hardware data protection is provided via the WP pin to protect against inadvertent write attempts to the status register. The HOLD pin may be used to suspend any serial communication without resetting the serial sequence.

The Pm25LV512/010 are manufactured on PMC's advanced nonvolatile CMOS technology, P-FLASH™. The devices are offered in 8-pin JEDEC SOIC and 8-contact WSON packages with operation frequency up to 25 MHz.

CONNECTION DIAGRAMS



8-Pin SOIC

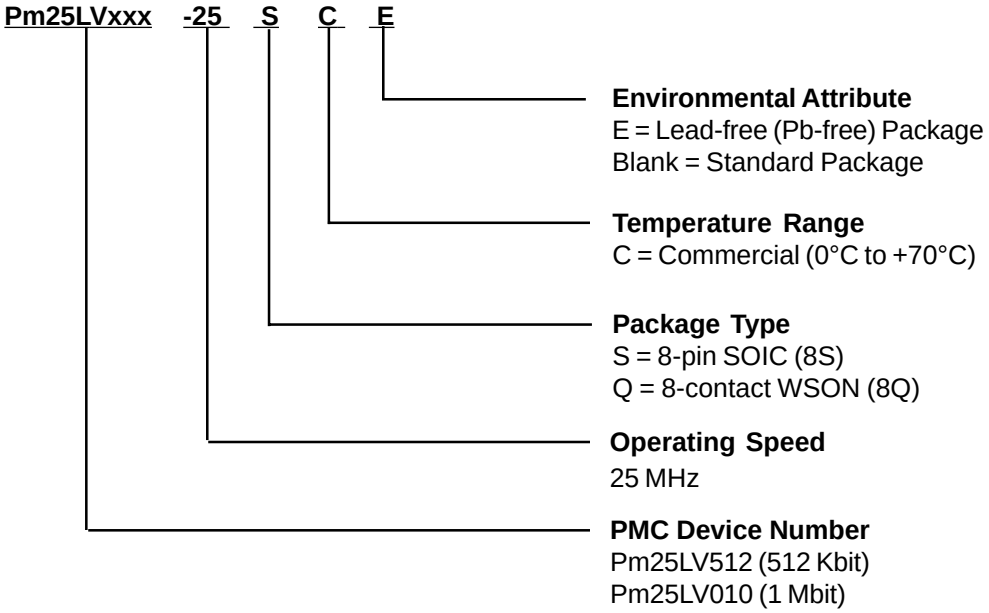


8-Contact WSON

PIN DESCRIPTIONS

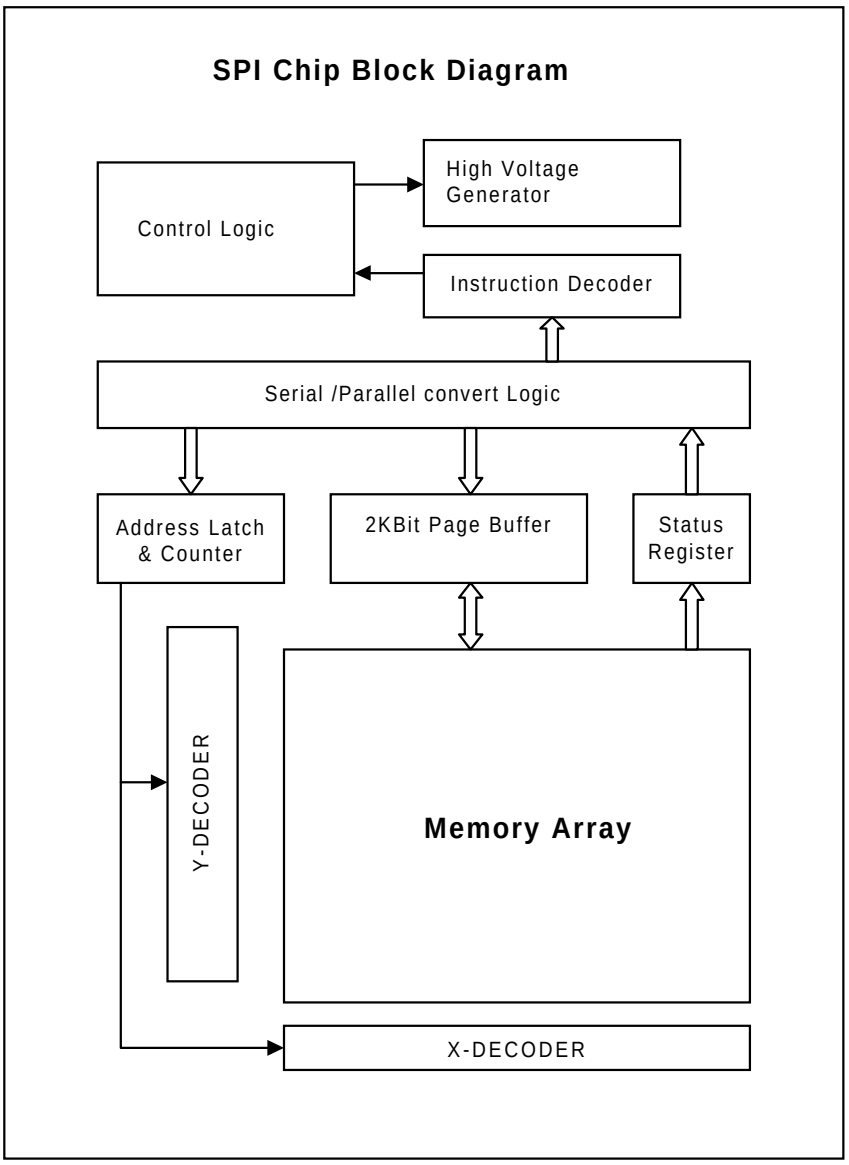
SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# goes low activates the device's internal circuitries for device operation. CE# goes high deselects the device and switches into standby mode to reduce the power consumption. When the device is not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SI	INPUT	Serial Data Input
SO	OUTPUT	Serial Data Output
GND		Ground
Vcc		Device Power Supply
WP#	INPUT	Write Protect: When the WP# pin brought to low and WPEN bit is "1", all write operations to the status register are inhibited.
HOLD#	INPUT	Hold: Pause serial communication with the master device without resetting the serial sequence.

PRODUCT ORDERING INFORMATION



Part Number	Operating Frequency (MHz)	Package	Temperature Range
Pm25LV512-25SCE	25	8S	Commercial (0°C to + 70°C)
Pm25LV512-25SC			
Pm25LV512-25QCE		8Q	
Pm25LV512-25QC			
Pm25LV010-25SCE	25	8S	
Pm25LV010-25SC			
Pm25LV010-25QCE		8Q	
Pm25LV010-25QC			

BLOCK DIAGRAM



SERIAL INTERFACE DESCRIPTION

Pm25LV512/010 can be driven by a microcontroller on the SPI bus as shown in Figure 1. The serial communication term definitions are in the following section.

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the Pm25LV512/010 always operates as a slave.

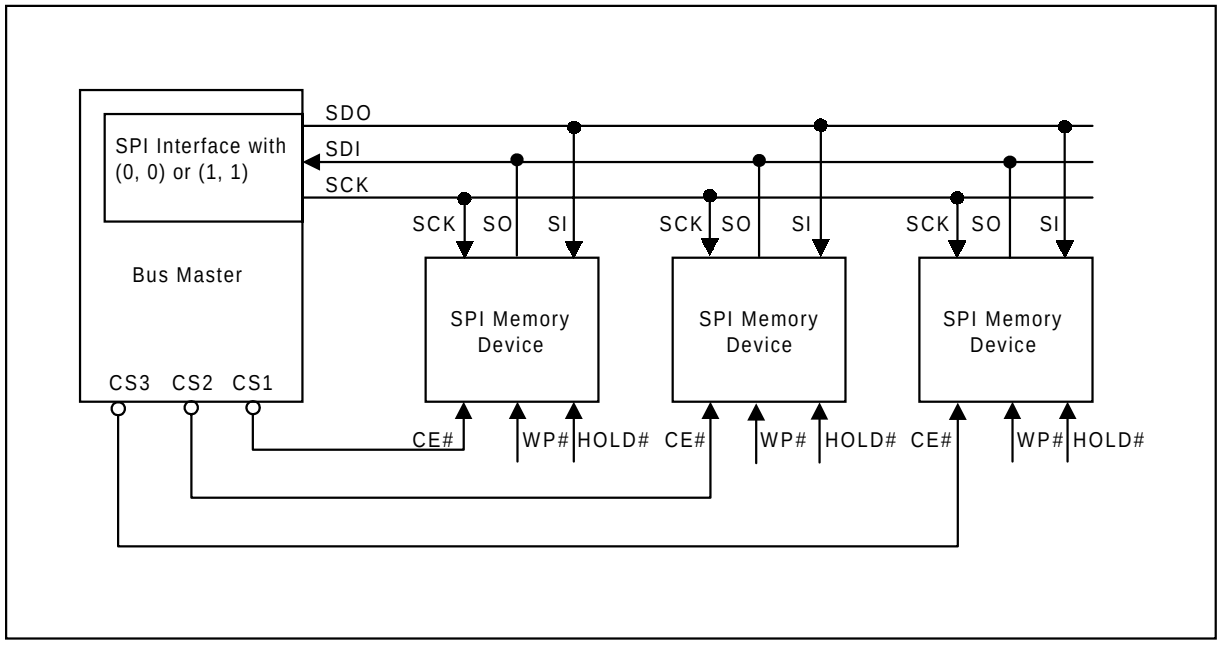
TRANSMITTER/RECEIVER: The Pm25LV512/010 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with CE# going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the Pm25LV512/010, and the serial output pin (SO) will remain in a high impedance state until the falling edge of CE# is detected again. This will reinitialize the serial communication.

Figure 1. Bus Master and SPI Memory Devices



Note: 1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven, High or Low as appropriate.

SERIAL INTERFACE DESCRIPTION (CONTINUED)

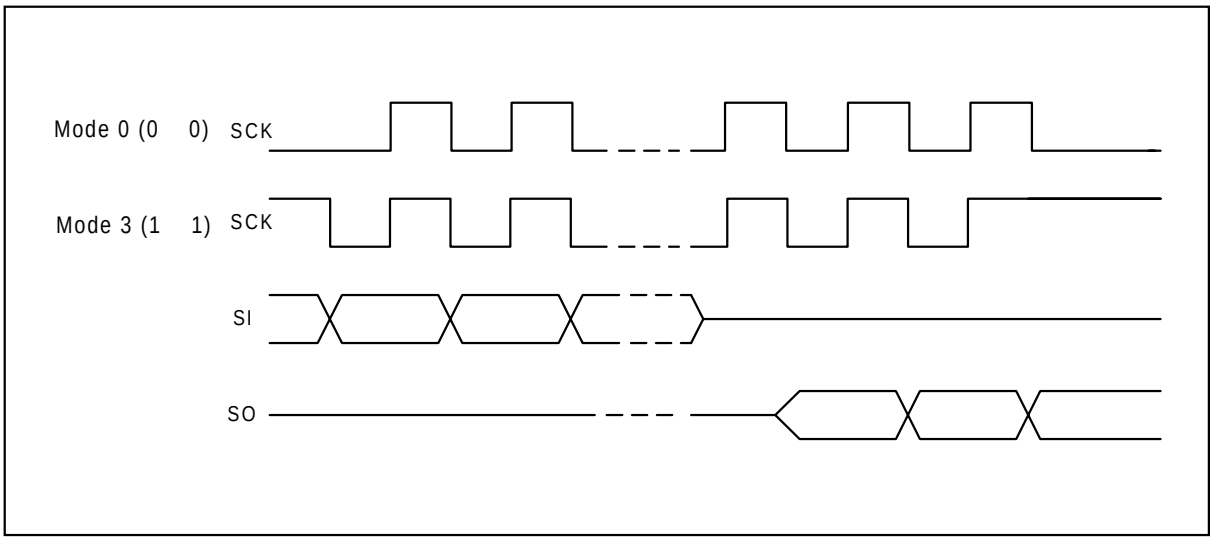
SPI MODES

These devices can be driven by microcontroller with its SPI peripheral running in either of the two following modes:
Mode 0 = (0, 0)
Mode 3 = (1, 1)

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Stand-by mode and not transfering data:
- Clock remains at 0 (SCK = 0) for Mode 0 (0, 0)
- Clock remains at 1 (SCK = 1) for Mode 3 (1, 1)

Figure 2. SPI Modes



DEVICE OPERATION

The Pm25LV512/010 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The Pm25LV512/010 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Write is defined as program and/or erase in this specification. The following commands, PAGE PROGRAM, SECTOR ERASE, BLOCK ERASE, CHIP ERASE, and WRSR are write instructions for Pm25LV512/010.

Table 1. Instruction Set for the Pm25LV512/010

Instruction Name	Instruction Format	Hex Code	Operation
WREN	0000 0110	06h	Set Write Enable Latch
WRDI	0000 0100	04h	Reset Write Enable Latch
RDSR	0000 0101	05h	Read Status register
WRSR	0000 0001	01h	Write Status Register
READ	0000 0011	03h	Read Data from Memory Arrary
FAST_READ	0000 1011	0Bh	Read Data from Memory at Higher Speed
PG_ PROG	0000 0010	02h	Program Data Into Memory Array
SECTOR_ERASE	1101 0111	D7h	Erase One Sector in Memory Array
BLOCK_ERASE	1101 1000	D8h	Erase One Block in Memory Array
CHIP_ERASE	1100 0111	C7h	Erase Entire Memory Array
RDID	1010 1011	ABh	Read Manufacturer and Product ID

READ PRODUCT ID (RDID): The RDID instruction allows the user to read the manufacturer and product ID of the device. The instruction code is followed by three dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then the first manufacturer ID (9Dh) is shifted out on Serial Data Output (SO), followed by the device ID (7Bh = Pm25LV512; 7Ch = Pm25LV010) and the second manufacturer ID (7Fh), each bit been shifted out during the falling edge of Serial Clock (SCK).

Table 2. Product Identification

Product Identification	Data
Manufacturer ID	9Dh
Device ID:	
Pm25LV512	7Bh
Pm25LV010	7Ch

WRITE ENABLE (WREN): The device will power up in the write disable state when Vcc is applied. All write instructions must therefore be preceded by the WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the WRDI instruction disables all write commands. The WRDI instruction is independent of the status of the WP# pin.

READ STATUS REGISTER (RDSR): The RDSR instruction provides access to the status register. The READY/BUSY and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction. During internal write cycles, all other commands will be ignored except the RDSR instruction.

Table 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	RDY

Table 4. Read Status Register Bit Definition

Bit	Definition
Bit 0 (RDY)	Bit 0 = 0 indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress and the device is BUSY.
Bit 1 (WEN)	Bit 1 = 0 indicates the device is not WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 5.
Bit 3 (BP1)	See Table 5.
Bits 4-6 are 0s when device is not in an internal write cycle.	
Bit 7 (WPEN)	WPEN = 0 blocks the function of Write Protect pin (WP#). WPEN = 1 activates the Write Protect pin (WP#). See Table 6 for details.
Bits 0-7 are 1s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection for the Pm25LV010. The Pm25LV010 is divided into four blocks where the top quarter (1/4), top half (1/2), or all of the memory blocks can be protected (locked out) from write. The Pm25LV512 is divided into 2 blocks where all of the memory blocks can be protected (locked out) from write. Any of the locked-out blocks will therefore be READ only. The locked-out block and the corresponding status register control bits are shown in Table 5.

The three bits, BP0, BP1, and WPEN, are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, RDSR).

Table 5. Block Write Protect Bits

Level	Status Register Bits		Pm25LV512		Pm25LV010	
	BP1	BP0	Array Addresses Locked Out	Locked-out Block(s)	Array Addresses Locked Out	Locked-out Block(s)
0	0	0	None	None	None	None
1(1/4)	0	1			018000 - 01FFFF	Block 4
2(1/2)	1	0			010000 - 01FFFF	Block 3, 4
3(All)	1	1	000000-00FFFF	All Blocks (1 - 2)	000000 - 01FFFF	All Blocks (1 - 4)

The WRSR instruction also allows the user to enable or disable the Write Protect (WP#) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the WP# pin is low and the WPEN bit is "1". Hardware write protection is disabled when either the WP# pin is high or the WPEN bit is "0." When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the locked-out blocks in the memory array are disabled. Write is only allowed to blocks of the memory which are not locked out. The WRSR instruction is self-timed to automatically erase and program BP0, BP1, and WPEN bits. In order to write the status register, the device must first be write enabled via the WREN instruction. Then, the instruction and data for the three bits are entered. During the internal write cycle, all instructions will be ignored except RDSR instructions. The Pm25LV512/010 will automatically return to write disable state at the completion of the WRSR cycle.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the WP# pin is held low.

Table 6. WPEN Operation

WPEN	WP	WEN	ProtectedBlocks	UnprotectedBlocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ: Reading the Pm25LV512/010 via the SO (Serial Output) pin requires the following sequence. After the CE# line is pulled low to select a device, the READ instruction is transmitted via the SI line followed by the byte address to be read (Refer to Table 7). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the CE# line should be driven high after the data comes out. The READ instruction can be continued since the byte address is automatically incremented and data will continue to be shifted out. For the Pm25LV512/010, when the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous READ instruction.

FAST_READ: The device is first selected by driving CE# low. The FAST READ instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCK (Serial Clock). Then the memory contents, at that address, is shifted out on SO (Serial Output), each bit being shifted out, at a maximum frequency f_{FR}, during the falling edge of SCK (Serial Clock).

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read with a single FAST READ instruction. The FAST READ instruction is terminated by driving CE# high.

PAGE PROGRAM (PG_PROG): In order to program the Pm25LV512/010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the PAGE PROGRAM instruction can be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal self-timed programming cycle, all commands will be ignored except the RDSR instruction.

The PAGE PROGRAM instruction requires the following sequence. After the CE# line is pulled low to select the device, the PAGE PROGRAM instruction is transmitted via the SI line followed by the address and the data (D7-D0) to be programmed (Refer to Table 7). Programming will start after the CE# pin is brought high. The low-to-high transition of the CE# pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a RDSR instruction. If Bit 0 = 1, the program cycle is still in progress. If Bit 0=0, the program cycle has ended. Only the RDSR instruction is enabled during the program cycle. A single PROGRAM instruction programs 1 to 256 consecutive bytes within a page if it is not write protected. The starting byte could be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged. If more than 256 bytes of data are provided, the address counter will roll over on the same page and the previous data provided will be replaced. The same byte cannot be reprogrammed without erasing the whole sector/block first. The Pm25LV512/010 will automatically return to the write disable state at the completion of the PROGRAM cycle.

Note: If the device is not write enabled (WREN) the device will ignore the Write instruction and will return to the standby state, when CE# is brought high. A new CE# falling edge is required to re-initiate the serial communication.

Table 7. Address Key

Address	Pm25LV512	Pm25LV010
A_N	A_{15} - A_0	A_{16} - A_0
Don't Care Bits	A_{23} - A_{16}	A_{23} - A_{17}

SECTOR_ERASE, BLOCK_ERASE: Before a byte can be reprogrammed, the sector/block which contains the byte must be erased. In order to erase the Pm25LV512/010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the SECTOR ERASE or BLOCK ERASE instruction can be executed.

Table 8. Block Addresses

Block Address	Pm25LV512 Block	Pm25LV010 Block
000000 to 007FFF	Block 1	Block 1
008000 to 00FFFF	Block 2	Block 2
010000 to 017FFF	N/A	Block 3
018000 to 01FFFF	N/A	Block 4

The BLOCK ERASE instruction erases every byte in the selected block if the block is not locked out. Block address is automatically determined if any address within the block is selected. The BLOCK ERASE instruction is internally controlled; it will automatically be timed to completion. During this time, all commands will be ignored, except RDSR instruction. The Pm25LV512/010 will automatically return to the write disable state at the completion of the BLOCK ERASE cycle.

CHIP_ERASE: As an alternative to the SECTOR and BLOCK ERASE, the CHIP ERASE instruction will erase every byte in all blocks that are not locked out. First, the device must be write enabled via the WREN instruction. Then the CHIP ERASE instruction can be executed. The CHIP ERASE instruction is internally controlled; it will automatically be timed to completion. The CHIP ERASE cycle time maximum is 100 miliseconds. During the internal erase cycle, all instructions will be ignored except RDSR. The Pm25LV512/010 will automatically return to the write disable state at the completion of the CHIP ERASE.

HOLD: The HOLD# pin is used in conjunction with the CE# pin to select the Pm25LV512/010. When the device is selected and a serial sequence is underway, HOLD# pin can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the HOLD# pin must be brought low while the SCK pin is low. To resume serial communication, the HOLD# pin is brought high while the SCK pin is low (SCK may still toggle during HOLD). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

HARDWARE WRITE PROTECT: The Pm25LV512/010 has a write lockout feature that can be activated by asserting the write protect pin (WP#). When the lockout feature is activated, locked-out sectors will be READ only. The write protect pin will allow normal read/write operations when held high. When the WP# is brought low and WPEN bit is "1", all write operations to the status register are inhibited. WP# going low while CE# is still low will interrupt a write to the status register. If the internal status register write cycle has already been initiated, WP# going low will have no effect on any write operation to the status register. The WP# pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the Pm25LV512/010 in a system with the WP# pin tied to ground and still be able to write to the status register. All WP# pin functions are enabled when the WPEN bit is set to "1".

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias		-65°C to +125°C
Storage Temperature		-65°C to +125°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins (2)		-0.5 V to V_{CC} + 0.5 V
All Output Voltage with Respect to Ground		-0.5 V to V_{CC} + 0.5 V
V_{CC} (2)		-0.5 V to +6.0 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are V_{CC} + 0.5 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number	**Pm25LV512/010**
Operating Temperature	0°C to 70°C
Vcc Power Supply	2.7 V - 3.6 V

DC CHARACTERISTICS

Applicable over recommended operating range from:
T_{AC} = 0°C to +70°C, V_{CC} = +2.7 V to +3.6 V (unless otherwise noted).

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC1}	Vcc Active Read Current	V_{CC} = 3.6V at 25 MHz, SO = Open			10	15	mA
I_{CC2}	Vcc Program/Erase Current	V_{CC} = 3.6V at 25 MHz, SO = OPen			15	30	mA
I_{SB1}	Vcc Standby Current CMOS	V_{CC} = 3.6V, CE# = V_{CC}			0.1	5	µA
I_{SB2}	Vcc Standby Current TTL	V_{CC} = 3.6V, CE# = V_{IH} to V_{CC}			0.05	3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C				1	µA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input HIgh Voltage			0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	2.7V < VCC < 3.6V	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

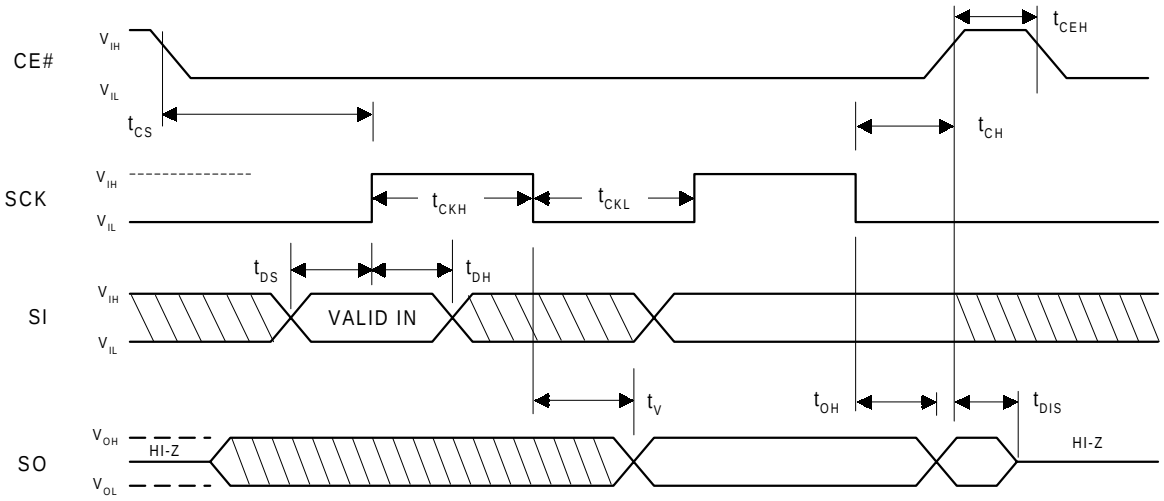
AC CHARACTERISTICS

Applicable over recommended operating range from T_A = 0°C to +70°C, V_{CC} = +2.7 V to +3.6 V
C_L = 1TTL Gate and 30 pF (unless otherwise noted).

Symbol	Parameter	Min	Typ	Max	Units
f_{FR}	Clock Frequency for FAST_READ	0		25	MHz
f_R	Clock Frequency for READ instructions	0		20	MHz
t_{RI}	Input Rise Time			20	ns
t_{FI}	Input Fall Time			20	ns
t_{CKH}	SCK High Time	20			ns
t_{CKL}	SCK Low Time	20			ns
t_{CEH}	CE High Time	25			ns
t_{CS}	CE Setup Time	25			ns
t_{CH}	CE Hold Time	25			ns
t_{DS}	Data In Setup Time	5			ns
t_{DH}	Data in Hold Time	5			ns
t_{HS}	Hold Setup Time	15			ns
t_{HD}	Hold Time	15			ns
t_V	Output Valid			15	ns
t_{OH}	Output Hold Time	0			ns
t_{LZ}	Hold to Output Low Z			200	ns
t_{HZ}	Hold to Output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{EC}	Secter/Block/Chip Erase Time		40	100	ms
t_{pp}	Page Program Time		2	5	ms
t_w	Write Status Register time		40	100	ms

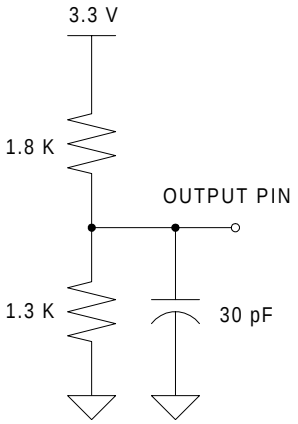
AC CHARACTERISTICS (CONTINUED)

AC WAVEFORMS(1)

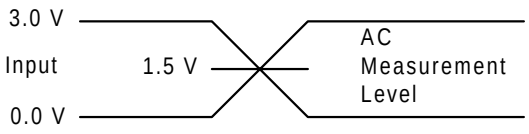


Note: 1. For SPI Mode 0 (0,0)

OUTPUT TEST LOAD

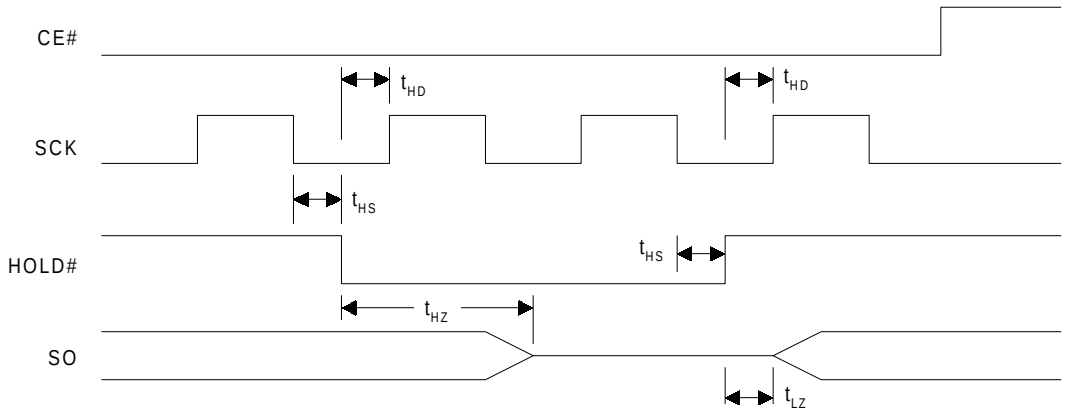


INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



AC CHARACTERISTICS (CONTINUED)

HOLD Timing



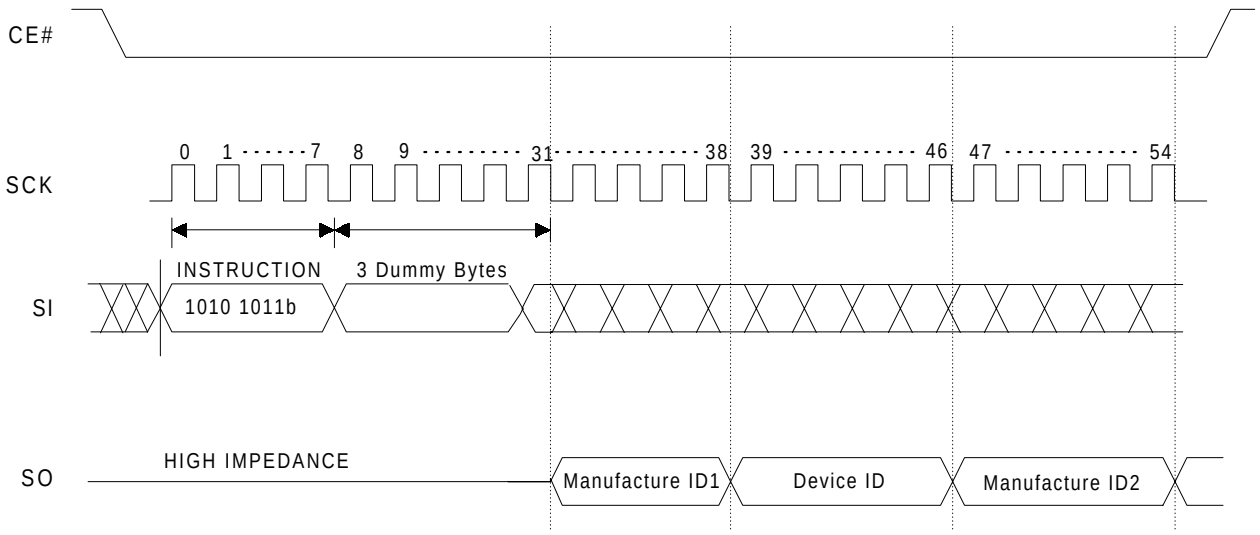
PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

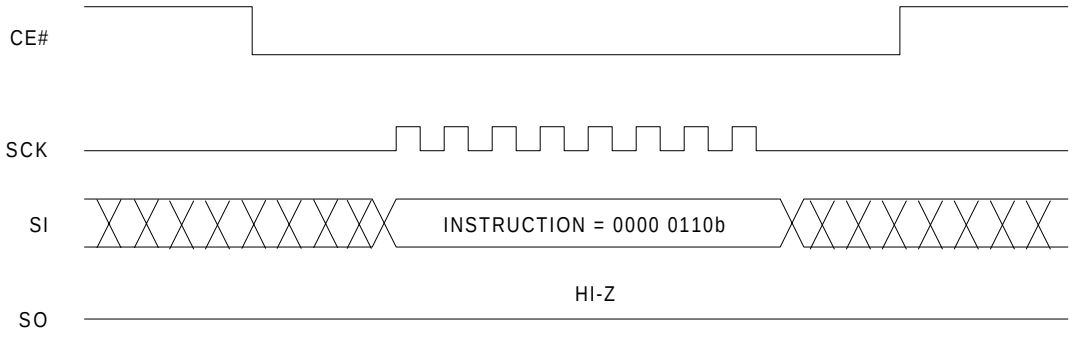
Note: These parameters are characterized but not 100% tested.

TIMING DIAGRAMS

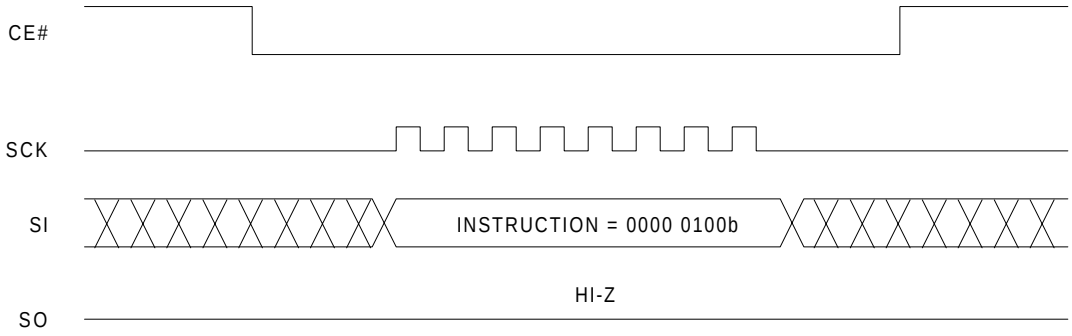
RDID Timing



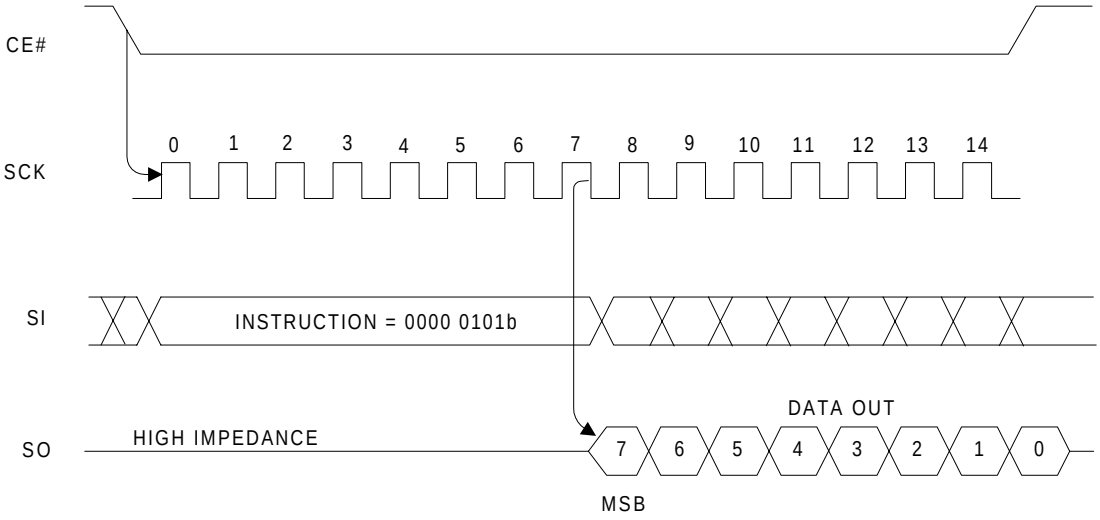
WREN Timing



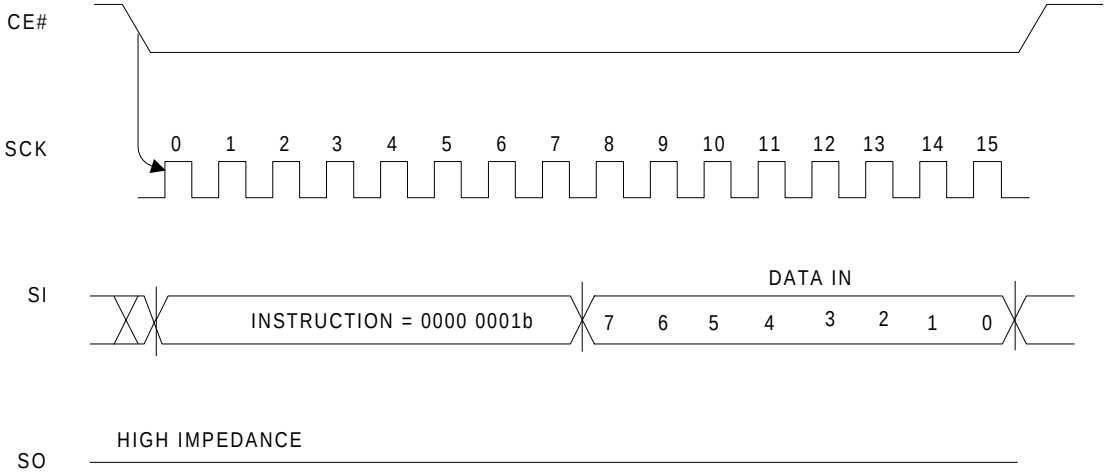
WRDI Timing



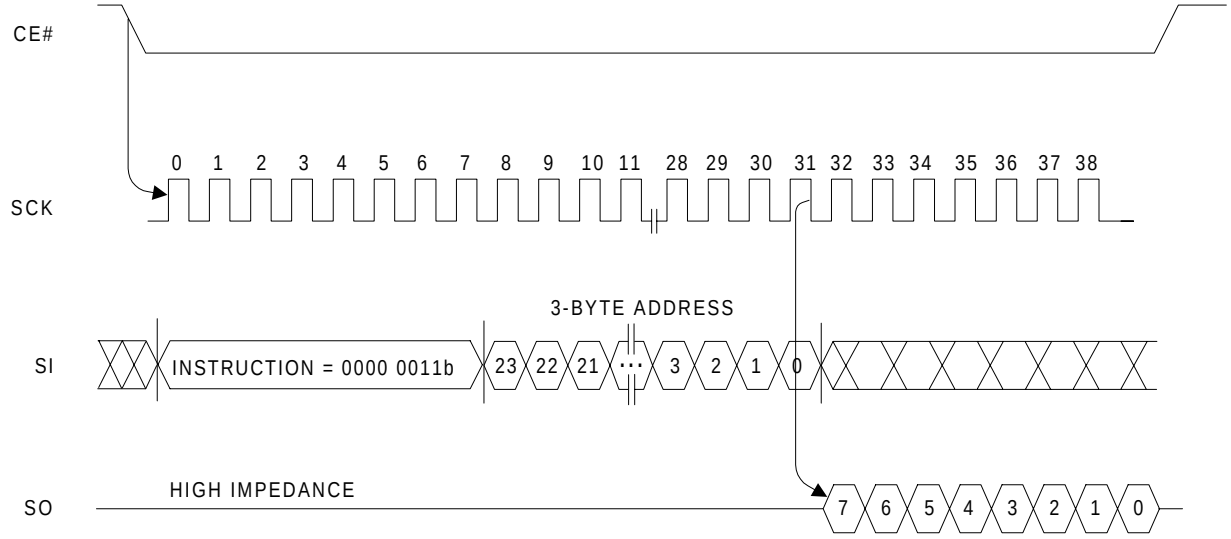
RDSR Timing



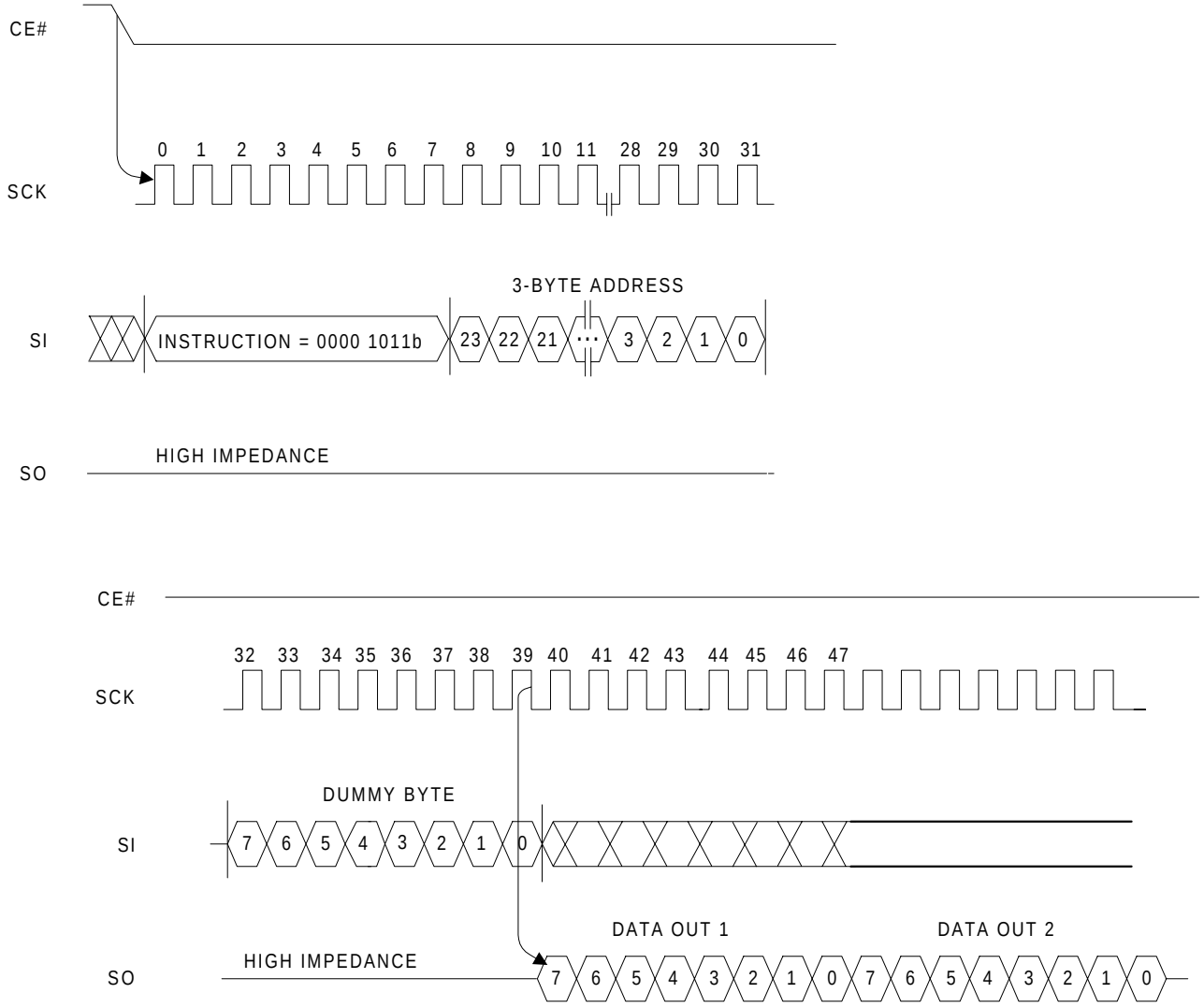
WRSR Timing



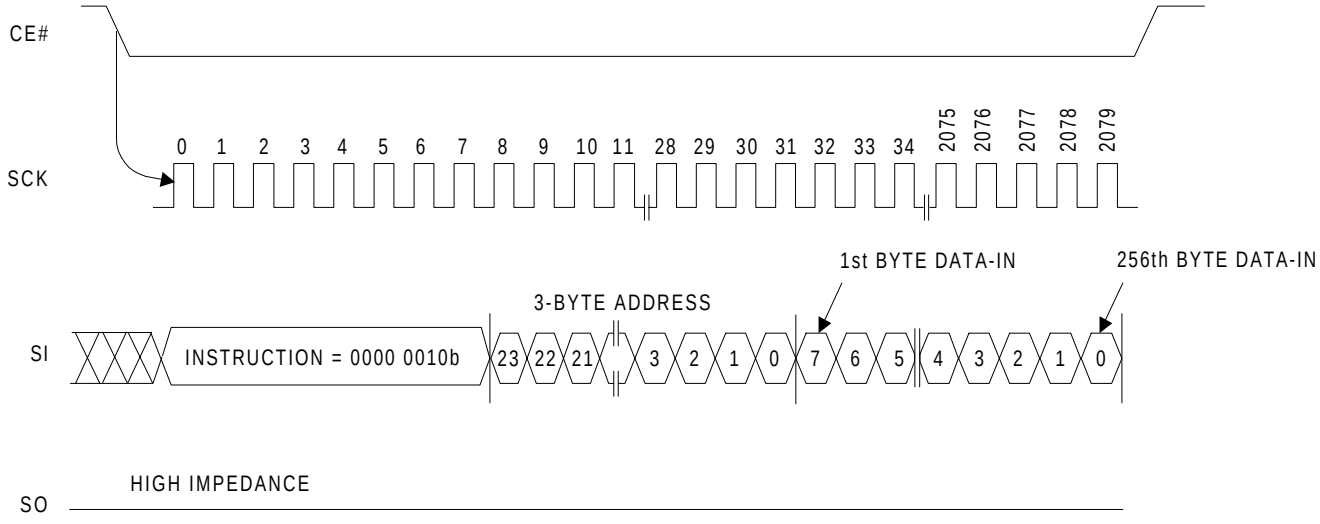
READ Timing



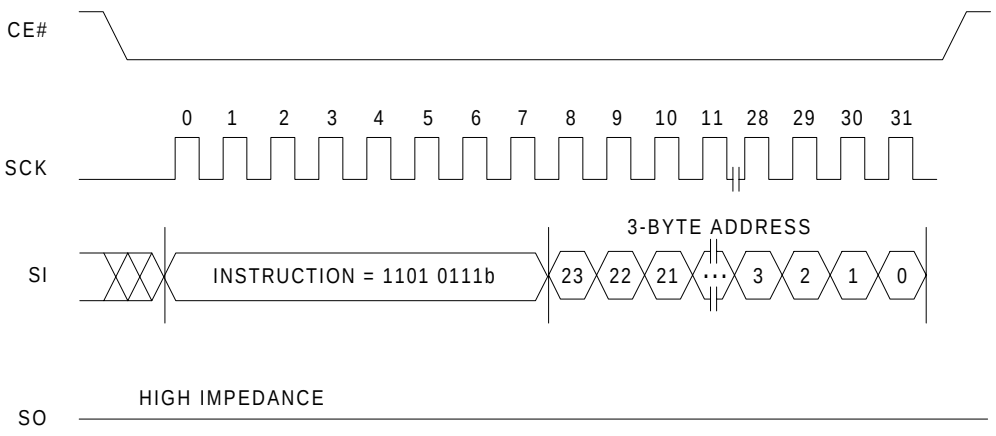
FAST READ Timing



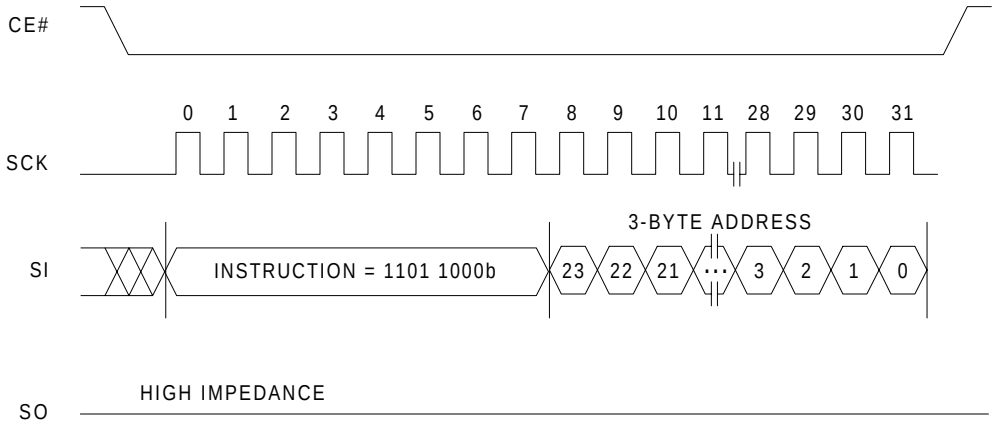
PAGE PROGRAM Timing



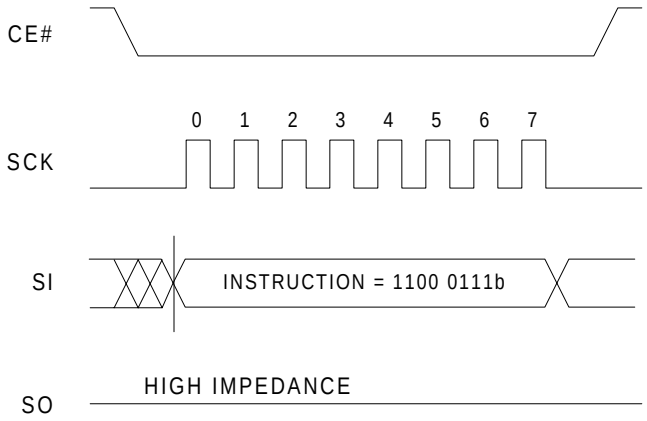
SECTOR ERASE Timing



BLOCK ERASE Timing



CHIP ERASE Timing



PROGRAM/ERASE PERFORMANCE

Parameter	Unit	Typ	Max	Remarks
Sector Erase Time	ms	40	100	From writing erase command to erase completion
Block Erase Time	ms	40	100	From writing erase command to erase completion
Chip Erase Time	ms	40	100	From writing erase command to erase completion
Page Programming Time	ms	2	5	From writing program command to program completion

Note: These parameters are characterized and are not 100% tested.

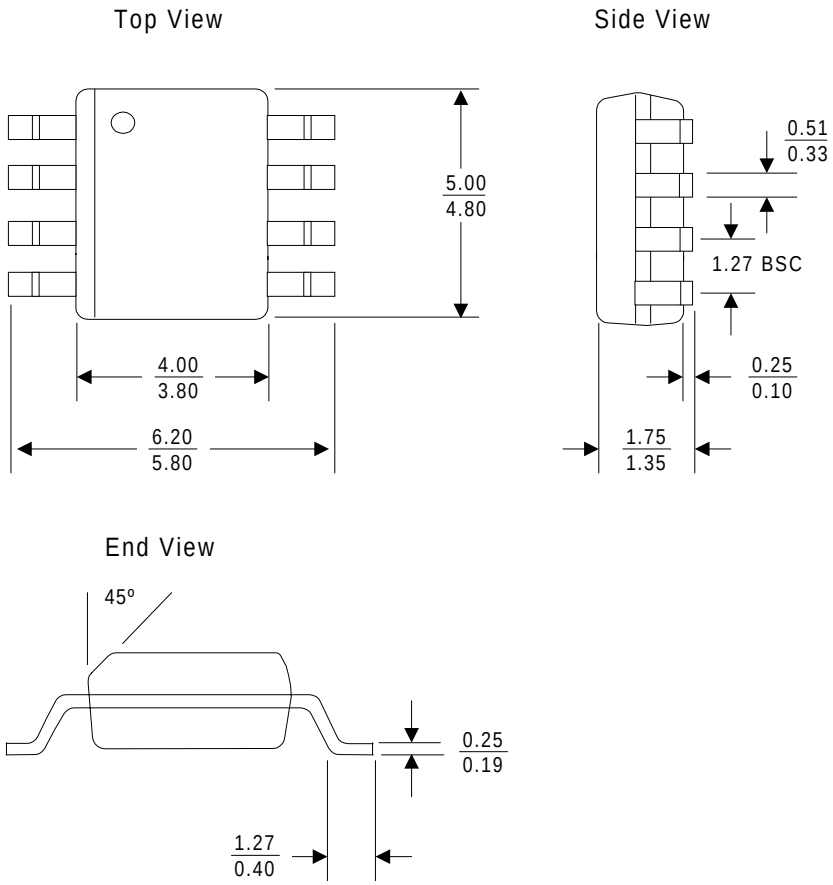
RELIABILITY CHARACTERISTICS (1)

Parameter	Min	Typ	Unit	Test Method
Endurance	100,000 (2)		Cycles	JEDEC Standard A117
Data Retention	20		Years	JEDEC Standard A103
ESD - Human Body Model	2,000		Volts	JEDEC Standard A114
ESD - Machine Model	200		Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}		mA	JEDEC Standard 78

Note: 1. These parameters are characterized and are not 100% tested.
2. Preliminary specification only and will be formalized after cycling qualification test.

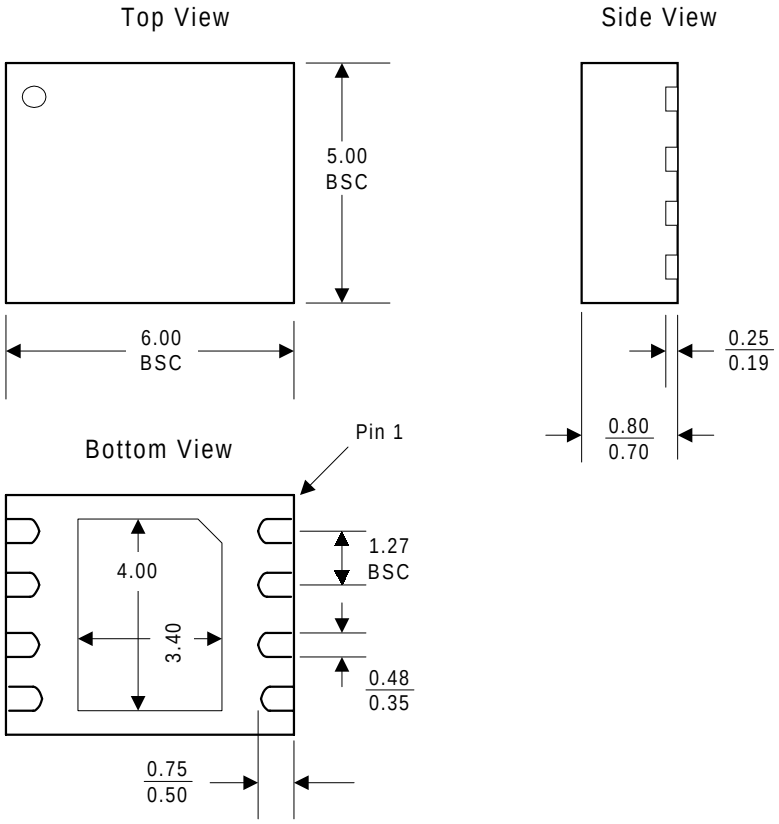
PACKAGE TYPE INFORMATION

8S
8-Pin JEDEC Small Outline Integrated Circuit (SOIC) Package (measure in millimeters)



PACKAGE TYPE INFORMATION (CONTINUED)

8Q
8-Contact Ulta-Thin Small Outline No-Lead (WSON) Package (measure in millimeters)



REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
October, 2002	1.0	New publication, Preliminary Spec	All
December, 2002	1.1	Formal Release	All
Jun, 2003	1.2	Added WSON package option	1, 2, 3, 23
December, 2003	1.3	Added Lead-free package options	1, 3, 12
		Upgraded guranteed program/erase cycles from 50,000 to 100,000 (preliminary)	1, 21
		Updated and redrawed package dimension	22, 23